Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) Method for making a field effect transistor comprising a source and a drain connected by a channel controlled by a gate electrode separated from the channel by a gate insulator, the channel being formed ~~by~~ in a diamond-like carbon layer, method successively comprising

- deposition of ~~a~~ said diamond-like carbon layer on a substrate,

- deposition of an insulating gate layer on the diamond-like carbon layer,

- deposition, on the insulating gate layer, of at least one conducting layer and etching of the latter so as to form the gate electrode,

- deposition of an insulating material on flanks of the gate electrode to form a lateral insulator,

- etching of the gate insulating layer,

- etching of the diamond-like carbon layer so as to delineate the channel, in said diamond-like carbon layer,

- deposition, on each side of the channel, of a semi-conducting material designed to form the source and of a semi-conducting material designed to form the drain.

2. (Previously Presented) Method according to claim 1, wherein etching of the diamond-like carbon layer is isotropic so as to obtain a retraction of the diamond-like carbon layer under the gate insulating layer.

3. (Previously Presented) Method according to claim 2, comprising anisotropic etching of the semi-conducting materials in the zones of the substrate not covered by the gate electrode and the lateral insulator.

4. (Previously Presented) Field effect transistor comprising a channel formed by a diamond-like carbon layer, transistor obtained by a method according to claim 1.

5. (Previously Presented) Transistor according to claim 4, wherein the channel comprises N-type dopants so as to form a PMOS type transistor.

6. (Previously Presented) Transistor according to claim 4, wherein the channel comprises P-type dopants so as to form a NMOS type transistor.

7. (Previously Presented) CMOS logic gate, comprising at least one PMOS type transistors according to claim 5 and at least one NMOS type transistor, the PMOS and NMOS type transistors having substantially the same dimensions.

8. (Previously Presented) CMOS logic gate, comprising at least one PMOS type transistor and at least one NMOS type transistor according to claim 6, the PMOS and NMOS type transistors having substantially the same dimensions.